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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,314	04/21/2004	Shekar Mallikarjunaswamy	M076P1	5669

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EXAMINER	
QUINTO, KEVIN V	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/829,314	MALLIKARJUNASWAMY, SHEKAR	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-16 and 18-22 have been considered but are moot in view of the new ground(s) of rejection.

Terminal Disclaimer

2. The terminal disclaimer filed on July 26, 2005 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of USPN 6,818,950 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 18-22 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a cellular power MOSFET array having source and drain electrical connection vias, does not reasonably provide enablement for a cellular power MOSFET array having source and drain electrical connection vias put through a field isolation layer. The specification does not enable any person skilled in

the art to which it pertains, or with which it is most nearly connected, to make or use the invention commensurate in scope with these claims.

5. Claim 18 has the limitation "...superjacent said surface layer, a field isolation layer, having source and drain electrical connection vias therethrough..." in lines 6-7 of the claim. However the examiner is unable to find any embodiment within the specification in which source and drain electrical connection vias are placed through a field isolation layer. The examiner has interpreted this limitation to mean that the source and drain electrical connection vias are placed through an interlayer dielectric formed over the top surface of the substrate.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 5 recites the limitation "the field isolation layer" in line 2. There is insufficient antecedent basis for this limitation in the claim.

9. Claims 20 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. The term "relative thick" in claims 20 and 22 is a relative term which renders the claim indefinite. The term "relative thick" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary

skill in the art would not be reasonably apprised of the scope of the invention. The term "relative thick" is not described in the specification with any kind of tolerance that would allow one to ascertain as to what is *relatively thick*.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 7-10, 12, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishida (JP 11-261056).

13. In reference to claim 7, Ishida (JP 11-261056) discloses a structure which meets the claim. Figures 6(a)-6(c) of Ishida illustrate a MOSFET array comprising a semiconductor material (10) having a top surface. There is a plurality of lateral metal-oxide-semiconductor transistors in a cellular array configuration with respect to the top surface. Each of the transistors includes a first region of a geometric gate construction (32) which overlies and is insulated from the top surface proximate a transistor channel region between a transistor source region (20) and a transistor drain region (22) in the top surface. The gate construction (32) forms a mesh having a plurality of substantially identical openings. Each of the openings approximates a predetermined geometric shape. An inherent capacitance-reducing plug (26) is subjacent each intersection of the mesh. The intersection forms a second region of the geometric gate construction (32)

which overlies and is insulated from the top surface proximate a third region of the top surface which intervenes adjacent source regions (20) and adjacent drain regions (22) of the transistors.

14. In reference to claim 8, the capacitance-reducing plug (26) is a volume of oxide (paragraph 15).

15. With regard to claim 9, the volume of oxide (26) has a geometric shape and geometric dimensions substantially conformed to the geometric shape and geometric dimensions of the intersection.

16. In reference to claim 10, the volume of oxide (26) extends from a bottom surface of the gate construction (32) into a predetermined depth of the top surface associated with the source region (20) and drain region (22) depth measured from the top surface into the semiconductor material (10).

17. In reference to claim 12, the capacitance-reducing plug (26) is a filled shallow trench isolation region.

18. With regard to claim 13, the geometric gate construction (32) is isolated from the top surface by a gate oxide layer (28). The capacitance-reducing plug (26) is a layer of capacitance-reducing material floating in the gate oxide layer (28) superjacent the top surface.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 1, 2, 3, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida (JP 11-261056) in view of Noble et al. (United States Patent Application Publication No. US 2002/0014660 A1).

21. In reference to claim 1, Ishida (JP 11-261056) discloses a structure which meets the claim. Figures 6(a)-6(c) of Ishida illustrate a cellular metal-oxide-semiconductor structure having a plurality of individual field effect transistors, the structure having a gate construction (32) having a predetermined geometric mesh configuration. Subjacent each intersection of the mesh is a substantially insulative material plug (26) which is inter-spaced between adjacent source regions (20) and adjacent drain regions (22) of the structure such that inherent capacitance is reduced (see abstract). Ishida does not disclose the use of a polysilicon gate material for the gate but the use of polysilicon as a gate material is well known in the art. Noble et al. (United States Patent Application Publication No. US 2002/0014660 A1, hereinafter referred to as the "Noble" reference) discloses that the use of a polysilicon gate in a transistor leads to a more reliable device with superior drains and sources (p. 1, paragraphs 4-5). In view of Noble, it would therefore be obvious to use polysilicon as the gate material in order to attain the benefit of a more reliable transistor.

22. In reference to claim 2, each of the plugs (26) is fabricated of a material for reducing capacitance between the gate constructions (32), the source regions (20) and the drain regions (22) of the structure (abstract, Ishida).

23. With regard to claim 3, each of the plugs (26) has a predetermined geometric shape and dimensions associated with gate length of each of the transistors.

24. With regard to claim 6, each of the plugs (26) is a filled shallow trench isolation region extending into a surface of the structure containing source regions (20) and drain regions (22) therein.

25. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida (JP 11-261056) in view of Noble et al. (United States Patent Application Publication No. US 2002/0014660 A1) as applied to claim 1 above and further in view of Hong (USPN 5,960,285).

26. In reference to claim 4, Ishida discloses the use of a plug (26) having a thickness greater than the gate oxide thickness for the transistors which extends from the gate structure into a substrate region interspaced between adjacent source (20) and drain (22) regions. Neither Ishida nor Noble discloses the use of a plug made of a field oxide region. However the use of field oxide regions is well known in the semiconductor art. Hong (USPN 5,960,285) discloses that field oxide regions have the benefits of a low cost while being reliable (column 4, lines 19-25). In view of Hong, it would therefore be obvious to implement a field oxide region.

27. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida (JP 11-261056) in view of Hong (USPN 5,960,285).

28. In reference to claim 11, Ishida discloses the use of a plug (26) but does not disclose the use of a plug made of a field oxide region. However the use of field oxide regions is well known in the semiconductor art. Hong (USPN 5,960,285) discloses that

field oxide regions have the benefits of a low cost while being reliable (column 4, lines 19-25). In view of Hong, it would therefore be obvious to implement a field oxide region.

29. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida (JP 11-261056) in view of Noble et al. (United States Patent Application Publication No. US 2002/0014660 A1) and further in view of Beyer (USPN 4,745,081).

30. With regard to claim 14, Ishida does not disclose the use of a poly-silicon having a first doping factor for the gate construction material but the use of polysilicon as a gate material is well known in the art. Noble (United States Patent Application Publication No. US 2002/0014660 A1) discloses that the use of a polysilicon gate having a first doping factor in a transistor leads to a more reliable device with superior drains and sources (p. 1, paragraphs 4-5). In view of Noble, it would therefore be obvious to use polysilicon as the gate material in order to attain the benefit of a more reliable transistor. Ishida does not disclose the use of a poly-silicon layer as the capacitance-reducing material in the plug. However the use of an insulative poly-silicon plug is well known in the semiconductor art. Beyer (USPN 4,745,081) discloses that insulative poly-silicon plugs have the benefit of being a low risk isolation scheme (column 1, lines 10-22). In view of Beyer, it would therefore be obvious to implement an insulative poly-silicon plug.

31. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida (JP 11-261056) in view of Noble et al. (United States Patent Application Publication No. US 2002/0014660 A1).

32. With regard to claim 15, Ishida discloses that the capacitance-reducing material (26) is silicon oxide which is a dielectric material (paragraph 15). Ishida does not

disclose the use of a poly-silicon having a first doping factor for the gate construction material but the use of polysilicon as a gate material is well known in the art. Noble (United States Patent Application Publication No. US 2002/0014660 A1) discloses that the use of a polysilicon gate having a first doping factor in a transistor leads to a more reliable device with superior drains and sources (p. 1, paragraphs 4-5). In view of Noble, it would therefore be obvious to use polysilicon as the gate material in order to attain the benefit of a more reliable transistor.

33. With regard to claim 16, Ishida teaches all of the claimed invention except for the exact thickness of the dielectric material. Although Ishida does not teach the exact thickness as that claimed by Applicant:

> Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).
>
> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Therefore claim 16 is not patentably distinguishable over the Ishida reference.

34. Claims 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida (JP 11-261056) in view of Noble et al. (United States Patent Application Publication No. US 2002/0014660 A1).

35. So far as understood in claim 18, Ishida (JP 11-261056) discloses a similar structure. Figures 6(a)-6(c) of Ishida illustrate a cellular power MOSFET integrated circuit comprising a semiconductor substrate (10) having a first ion doping type and a surface layer (10) which has an active element well having the first ion type doping.

There is an array of MOSFETs including at least one row of source regions (20) and at least one row of drain regions (22). Superjacent the surface layer (10) it is understood that there is an interlayer dielectric layer through which source and drain electrical connection vias are formed. There is a geometric gate construction 932) which forms a grid having a plurality of substantially identical openings of a predetermined geometric shape and dimensions. A gate oxide layer (28) separates the gate construction (32) from the surface layer (10). A capacitance-reducing plug (26) is at each intersection of the grid such that the plugs (26) are inter-spaced between adjacent source regions (20) of transistor source rows and adjacent drain regions (22) of transistor drain rows of each row of the array. Ishida does not disclose the use of a poly-silicon having a first doping factor for the gate construction material but the use of polysilicon as a gate material is well known in the art. Noble (United States Patent Application Publication No. US 2002/0014660 A1) discloses that the use of a polysilicon gate having a first doping factor in a transistor leads to a more reliable device with superior drains and sources (p. 1, paragraphs 4-5). In view of Noble, it would therefore be obvious to use polysilicon as the gate material in order to attain the benefit of a more reliable transistor.

36. So far as understood in claim 21, each of the plugs (26) is a trench isolation insulator.

37. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida (JP 11-261056) in view of Noble et al. (United States Patent Application Publication No. US 2002/0014660 A1) as applied to claim 18 above and further in view of Hong (USPN 5,960,285).

38. So far as understood in claim 19, neither Ishida nor Noble discloses the use of a plug made of a field oxide region. However the use of field oxide regions is well known in the semiconductor art. Hong (USPN 5,960,285) discloses that field oxide regions have the benefits of a low cost while being reliable (column 4, lines 19-25). In view of Hong, it would therefore be obvious to implement a field oxide region.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KVQ

LEONARDO ANDUJAR
PRIMARY EXAMINER